AMENDMENT(S) TO THE CLAIMS

1. (Currently Amended) A memory ~~device~~ controller comprising:

~~a plurality of dynamically refreshable memory cells;~~

~~self refresh~~ refresh logic to refresh ~~the~~ memory cells of at least one memory device; and

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells of the at least one memory device, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use ~~and wherein the use registers and the self refresh logic are implemented in a same device as the memory cells~~;

wherein the refresh logic ~~memory device~~ is configured to omit refreshing of memory cells that are not in use.

2. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, wherein the ~~self refresh~~ refresh logic on the memory ~~device~~ controller is configured to not refresh the indicated unused groups of memory cells.

3. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory ~~device~~ controller is configured to omit refreshing of those memory cells that are indicated

by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

4. (Currently Amended) A system comprising ~~a plurality of memory devices~~ the memory controller as recited in claim 1, further comprising a plurality of memory devices, which include the at least one memory device, that comprise the groups of memory cells~~controller configured to set the use registers to indicate whether the memory cells are unused~~.

5. (Currently Amended) A system comprising ~~a plurality of memory devices~~ the memory controller as recited in claim 1, the system further comprising a plurality of memory devices that include recent-access flags configured to indicate whether associated sets of the memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval~~a memory controller implemented on a different device than the use registers~~.

6. (Currently Amended) A ~~system comprising a plurality of memory devices~~ memory controller as recited in claim 1, further comprising:

~~a memory controller configured to~~ a cache that is adapted to cache at least some of those memory cells that are indicated by the use registers to be in use and to omit refreshing of the cached memory cells.

7. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a set of memory cells.

8. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a row of memory cells.

9. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a bank of memory cells.

10. (Currently Amended) A memory ~~device~~ controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a page of memory cells.

11. (Currently Amended) A ~~memory device~~ system comprising:

a plurality of memory devices having memory cells; and

~~self-refresh logic to refresh the memory cells; and~~

a memory controller including one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are programmable to indicate whether the corresponding groups of memory cells are in use ~~and wherein the use registers and the self-refresh logic are implemented in a same device as the memory cells~~.

12. (Currently Amended) A ~~memory device~~ system as recited in claim 11, further comprising:

refresh logic that ~~wherein the self-refresh logic~~ is configured not to refresh unused memory cells.

13. (Currently Amended) A ~~memory device~~ system as recited in claim 11, further comprising:

recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the ~~memory device~~ system is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

14. (Currently Amended) A system ~~comprising a plurality of memory devices~~ as recited in claim ~~11~~ 13, wherein the recent-access flags are part of the plurality of memory devices~~further comprising a memory controller configured to program the use registers depending on whether the memory cells are being used~~.

15. (Currently Amended) A system ~~comprising a plurality of memory devices as recited in claim 11~~ as recited in claim 13, wherein the recent-access

flags are part of the ~~further comprising a~~ memory controller ~~that is implemented on a different device than the use registers~~.

16. (Currently Amended) A system ~~comprising a plurality of memory devices~~ as recited in claim 11, ~~further comprising a~~ wherein the memory controller ~~that~~ is configured to operate unused memory cells at reduced power.

17. (Currently Amended) A system ~~comprising a plurality of memory devices~~ as recited in claim 11, further comprising:

a cache that is adapted ~~memory controller configured~~ to cache at least some of those memory cells whose use registers indicate they are not unused;

wherein the memory controller is configured ~~and~~ to omit refreshing of the cached memory cells.

18. (Currently Amended) A ~~memory device~~ system as recited in claim 11, wherein the use registers comprise bits that each correspond to a row of memory cells.

19. (Currently Amended) A system comprising:

one or more memory devices having dynamically refreshable memory cells;

a memory controller having refresh logic configured to periodically refresh the memory cells of the memory devices;

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use;

wherein the refresh logic ~~on one of the memory devices~~ is further configured not to refresh memory cells that are not in use; and

recent-access flags associated with the memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the ~~memory controller~~ refresh logic is further configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval,

wherein the ~~refresh logic and the~~ use registers are not implemented on a same device as the memory cells.

20. (Currently Amended) A system as recited in claim 19, wherein the ~~use registers~~ recent-access flags are not implemented ~~on a different device than~~ as part of the memory controller.

21. (Currently Amended) A system as recited in claim 19, wherein the memory controller is configured to cache at least some of those memory cells that are not indicated by the one or more use registers to be unused; and wherein the refresh logic is further configured to omit refreshing of the cached memory cells.

22. (Canceled)

23. (Canceled)

24. (Original) A system as recited in claim 19, wherein the use registers comprise bits that each correspond to a row of memory cells.

25. (Currently Amended) A system comprising:

memory including one or more memory cells;

a memory controller;

an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller based on whether or not virtual-to-physical memory mapping portions are active; and

recent-access flags associated with the one or more memory cells~~and implemented on a same device as the memory cells~~, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the ~~memory controller~~ system is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval;

wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

26. (Original) A system as recited in claim 25, wherein the memory is dynamically refreshable memory and the memory controller operates the non-allocated memory at reduced power by omitting refreshing of non-allocated memory.

27. (Canceled)

28. (Currently Amended) A system as recited in claim 25, wherein the memory controller is configured to cache at least some of the allocated memory and to omit refreshing of the cached memory.

29. (Currently Amended) A system as recited in claim 25, further comprising:

a plurality of use bits corresponding respectively to memory rows, wherein each use bit ~~being~~ is configurable to indicate whether its corresponding memory row is currently allocated~~, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated~~.

30. (Original) A system as recited in claim 25, further comprising a plurality of use bits on the memory controller corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory

controller is configured to omit refreshing of memory rows that are not currently allocated.

31. (Currently Amended) A system as recited in claim 25, wherein the memory comprises a plurality of discrete memory devices, the system further comprising a plurality of use bits on the memory devices corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated by configuring the use bits.

32. (Currently Amended) In a system having dynamically refreshable memory rows, a method of memory power management, comprising:

indicating that memory rows, which have been transferred to a cache, are not in use upon transfer to the cache;

keeping track of which memory rows are in use and therefore need refreshing;

periodically refreshing those memory rows that are in use; and

omitting refreshing of memory rows that are not in use; ~~and~~

~~determining which rows have been accessed in a manner that refreshed the memory rows during a previous refresh cycle interval, wherein the determining act is performed by utilizing a plurality of recent access flags associated with each of the memory rows and implemented in a same device as the memory rows~~.

33. (Currently Amended) A method as recited in claim 32, further comprising:

determining which rows have been accessed in a manner that refreshed the memory rows during a previous refresh cycle interval, wherein the determining act is performed by utilizing a plurality of recent-access flags associated with each of the memory rows; and

omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory ~~cells~~ rows during the previous refresh cycle.

34. (Currently Amended) A method as recited in claim 32, ~~further comprising~~ wherein the indicating comprises resetting one or more use registers corresponding to the memory rows that have been transferred to the cache:

~~caching at least some of the memory rows that are in use; and~~

~~omitting refreshing of the cached memory rows~~.

35. (Original) A method as recited in claim 32, wherein keeping track comprises maintaining a plurality of flags corresponding respectively to the memory rows.

36. (Canceled)

37. (Canceled)

38. (Currently Amended) A memory controller configured to perform actions comprising:

periodically refreshing memory cells;

receiving internal notifications regarding which memory cells are in use based on data stored in a plurality of use registers located on the memory controller; and

omitting refreshing of those memory cells that are not in use~~; and~~

~~keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval;~~

~~wherein the keeping track action is performed by utilizing a plurality of recent access flags that are implemented adjacent to the memory cells;~~

~~wherein the memory controller is implemented in a different device than the use registers~~.

39. (Currently Amended) A memory controller as recited in claim 38, the memory controller being configured to perform further actions comprising:

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

40. (Currently Amended) A memory controller as recited in claim 38, the memory controller being configured to perform further actions comprising:

caching at least some of the memory cells that are in use; and

omitting refreshing of the cached memory cells.

41. (Canceled)

42. (Canceled)

43. (Canceled)

44. (Canceled)

45. (Canceled)

46. (Canceled)

47. (Canceled)

48. (Canceled)

49. (Canceled)

50. (Canceled)

51. (Canceled)

52. (Currently Amended) A method comprising:

receiving memory allocation and de-allocation notifications from an operating system;

periodically refreshing memory cells that are allocated;

omitting refreshing of memory cells that are de-allocated;

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle,

wherein the memory allocation and de-allocation notifications are based on virtual memory mapping portions~~period refreshing is performed by self-refresh logic and wherein the keeping track act is performed by utilizing a plurality of recent-access flags, the self refresh logic being implemented on a same device as the memory cells~~.

53. (Currently Amended) A ~~memory controller~~ method as recited in claim 52, further comprising:

responsive to the receiving, setting and unsetting ~~notifications regarding which memory cells are in use through a plurality of corresponding~~ use registers corresponding to memory addresses of the memory allocation and de-allocation notifications, respectively; ~~and~~

~~omitting refreshing of those memory cells that are not in use~~.

54. (Currently Amended) A system as recited in claim 19, wherein the use registers are implemented ~~on a different device than~~ as part of the memory controller.

55. (Currently Amended) A system as recited in claim 25, wherein the recent-access flags ~~memory cells~~ are located on ~~a different device than~~ the memory controller, and the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

56. (Currently Amended) A system as recited in claim 29, wherein the use bits are implemented ~~on a same device~~ as part of the memory cells or as part of the memory controller.

57. (Currently Amended) A method as recited in claim 34, further comprising:

flushing contents of the cache back to the memory rows; and

setting the one or more use registers corresponding to the memory rows to indicate that the memory rows are in use~~wherein a plurality of use registers are utilized to determine whether a memory row is in use and the use registers are implemented on the same device as the memory rows~~.

58. (Currently Amended) A memory controller as recited in ~~claim 38~~ claim 39, wherein the keeping track action is performed by utilizing a plurality of recent-access flags located on the memory controller~~use registers and the memory cells are implemented on a same device~~.

59. (Currently Amended) A ~~memory controller~~ method as recited in claim 53, wherein the setting and unsetting comprises setting and unsetting use registers that are implemented as part of a memory controller~~and the memory cells are implemented on the same device as the self refresh logic~~.